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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/700,940	11/21/2000	Shiro Sakiyama	10873.589USW	4531
7590	01/14/2004		EXAMINER	
Merchant & Gould PO Box 2903 Minneapolis, MN 55402-0903			EVERHART, CARIDAD	
			ART UNIT	PAPER NUMBER
			2825	

DATE MAILED: 01/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>
	09/700,940	SAKIYAMA ET AL.
	<b>Examiner</b>	Art Unit Caridad M. Everhart 2825

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) Responsive to communication(s) filed on \_\_\_\_\_.
- 2a) This action is FINAL.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) Claim(s) 1-6 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-6 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) The proposed drawing correction filed on \_\_\_\_\_ is: a) approved b) disapproved by the Examiner.  
 If approved, corrected drawings are required in reply to this Office action.
- 12) The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) All b) Some \* c) None of:
    1. Certified copies of the priority documents have been received.
    2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
  - a) The translation of the foreign language provisional application has been received.
- 15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

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|--|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                    | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ . |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)           | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ . | 6) <input type="checkbox"/> Other: _____ .                                   |

Applicant's arguments with respect to claims 1-6 have been considered but are moot in view of the new ground(s) of rejection.

Applicant's arguments are dependent upon applicant's amendments, and new prior art is applied below, as rejections based on the newly discovered prior art are necessitated by applicant's amendments.

***Claim Rejections - 35 USC § 112***

Claims 1 and 6 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The recitation "in combination" does not seem to be supported. In applicant's remarks, applicant pointed out the recitation "vicinity" as support; however, it does not seem that vicinity, which would indicate location, supports the recitation "in combination".

***Claim Rejections - 35 USC § 103***

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1, 3, 4, and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kinoshita (US 5,869,852) in view of Young(US 6,229,861B1).

Kinoshita discloses a method for layout of logic cells (col. 1, lines 10-15 and 36-40) and capacitors in cells between the logic cells and the power supply(col. 1, lines 42-46 and col. 2,lines 50-55). The capacitor cells are in the vicinity of the logic cells(col. 2,

lines 65-68 and col. 3, lines 1-3). Because Kinoshita teaches that the capacitor cells are between the logic cells(col. 4, lines 57-65), this is interpreted as that the cells are in areas where the logic cells are not arranged as required by claim 4. The arrangement is carried out by computer(col. 6, lines 53-59), so that the method is an automatic method. Although Kinoshita discloses logic cells rather than logic gate cells, logic cells are the same, because logic cells would be made up of logic gates. The number of capacitor cells is calculated based on the available space between the logic cells(col. 4, lines 57-65), as the disclosure of the dimensions of the capacitor cells being taken into account and the arranging of the cells in the spaces between the logic cells would involve the calculation of how many cells of these dimensions could be placed in the space.

Kinoshita is silent with respect to the capacitance corresponding to a drive load capacity of the logic gate cells, and the clock generation.

Young discloses that capacitance of the elements in a system are matched in order to eliminate delay(col. 2, lines 22-29 and col. 4, lines 43-50). This layout is in accordance with clock synchronization design.

It would have been obvious to one of ordinary skill in the art to have related the capacitance corresponding to a drive load capacity of the logic gate cells because Young discloses that it is known in the prior art to relate the capacitances of the logic components and the capacitors in order to eliminate delay. In addition, the arrangement would change in the layout depending on the clock synchronization design, in accordance with the disclosure made by Young, because Kinoshita teaches an

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automatic design method, which would arrange and size the capacitors with automatic design.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kinoshita in view of Young as applied to claim 1 above, and further in view of Kusunoki,k et al. ("Kusunoki") (US 5,512,766) .

Kinoshita in view of Young is silent with respect to the details of the power supply capacitance cell.

Kusunoki is relied upon for its teaching of the details of a unit capacitor cell which includes the n region and the polycrystalline silicon layer connected to the voltage source(col. 9, lines 49-64 and col. 10, lines 40-63).

It would have been obvious to one of ordinary skill in the art to have combined the teachings of Kusunoki with the device and method taught by Kinoshita in view of Young because the capacitor cell taught by Kusunoki can be made to provide the capacitance required for a capacitor from a voltage source to logic block cells (Kusunoki col. 3, lines 22-33).

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kinoshita in view of Young as applied to claim 1 above, and further in view of Mihara, et al. ("Mihara") (US 5,406,510).

Kinoshita in view of Young is silent with respect to the recited value of the capacitance. Mihara is relied upon for its teaching that the capacitance of the capacitors from a voltage source can be set to twice the value of the load(col. 1, lines 54-68), as the plate disclosed is the load.

It would have been obvious to one of ordinary skill in the art to have set the capacitance of the capacitor cells taught by Kinoshita in view of Young to twice the load capacity in view of the teaching of Mihara because this would decrease fluctuations in the voltage.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Caridad M. Everhart whose telephone number is 571-272-1892. The examiner can normally be reached on Monday through Fridays 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone

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numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

C. Everhart  
January 12, 2004

*C. Everhart*  
CARIDAD EVERHART  
PRIMARY EXAMINER